# Pulse Width Modulation Implementation using FPGA and CPLD ICs

Jakirhusen I. Tamboli, Prof. Satyawan R. Jagtap, Amol R. Sutar

**Abstract -** Pulse width modulation (PWM) has been widely used in power converter control. Most high power level converters operate at switching frequencies in excess of 1 MHz at high power levels can be achieved using the planar transformer technology. PWM control is the most powerful technique that offers a simple method for controlling of analog systems with processors digital output. The resulting PWM frequency depends on the target FPGA or CPLD device speed and duty cycle resolution requirements. The contribution of this paper is the development of high frequency PWM generator architecture for power converter control using FPGA and CPLD ICs.

**Index Terms -** Pulse width modulation, Field programmable gate array, CPLD, counter

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## 1 INTRODUCTION

The pulse width modulation (PWM) principle is widely used in power electronics applications for controlling power converters (DC/DC, DC/AC, etc.) Texas instruments TMS 320, F 2812 is used to generate PWM signals for single phase inverter. The PWM is widely used for motion control.

The PWM signal is generated by comparing an adjustable reference voltage, Vref, with a triangular wave of constant amplitude and frequency. The DC output voltage is regulated to the desired value by adjusting the reference voltage value, thus modifying the PWM signal duty cycle, as follows:

$$V_o = D \cdot V_{in} = \frac{t_{on}}{T_s} \cdot V_{in} = \frac{V_{ref}}{V_{tr}} \cdot V_{in}$$

where, $V_{in}$ is the converter DC input voltage, D is the PWM signal duty cycle ($0 \leq D \leq 1$), $t_{on}$ is the PWM signal ON time, $T_s$ is the converter switching period and $V_{tr}$ is the triangular wave amplitude.

The Sine Wave is used as a reference to generate PWM, because many AC Motors runs at 50 Hz supply, the 50 Hz Sine Wave ($V_m$) is generated using FPGA controller as shown in figure 1.1. The high frequency Triangular wave ($V_c$) shown in figure 1.2 is used as a carrier signal. This high frequency Triangular wave carrier signal is compared with a Sinusoidal reference signal. The crossover points are used to determine the switching instants such that if $V_{reference}$ is greater than $V_{carrier}$ then output is high otherwise output is low. The PWM output is shown in figure 1.3.

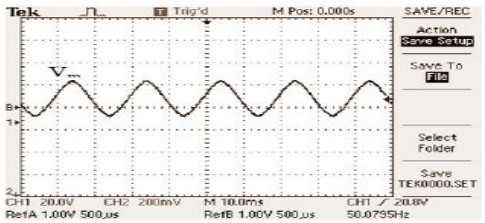


Fig.1.1: Sine wave

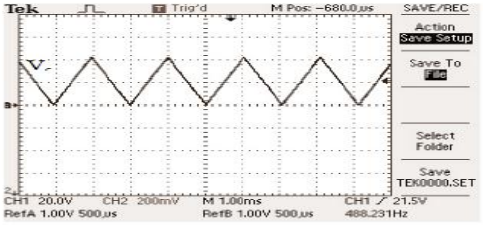


Fig.1.2: Triangular wave

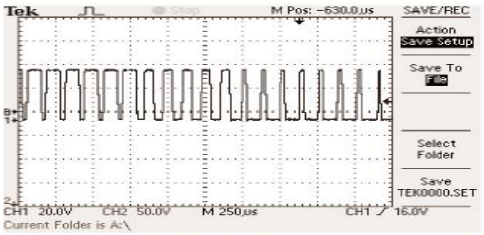


Fig.1.3: SPWM wave

The PWM control strategy has also been applied in zero voltage and zero current switching (ZVS and ZCS, respectively) resonant converters, which have the advantages of lower electromagnetic emission and higher operating frequency capability, compared to the hard-switching converter implementation. In all design methods, the switching frequency selection is a compromise between the power switch losses and the magnetic components power losses.

## 2 IMPLEMENTATION OF DIGITAL POWER CONVERTER CONTROL

In many applications it is desirable to control a power converter using a microcontroller or a digital signal processor (DSP) for the implementation of sophisticated control schemes such as fuzzy control [6], renewable energy sources control [7], etc. The block

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diagram of such a configuration is shown in Fig. 2(a). A set of sensors, used to measure the power converter signals of interest, such as the output current or voltage, output frequency, etc., are interfaced through an Analog to Digital (A/D) converter to a microcontroller or DSP unit.

The measured parameters are input to a digital controller in order to adjust the duty cycle value of the PWM signals, which further control the power converter operation, according to the desired control law, such as fuzzy logic control, PID control, neural networks control, etc. Since it is desirable to integrate all operations in a single IC for reduction of the total system cost, each PWM signal is usually generated using an on-chip PWM generator, built according to the general block diagram shown in Fig. 2(b).

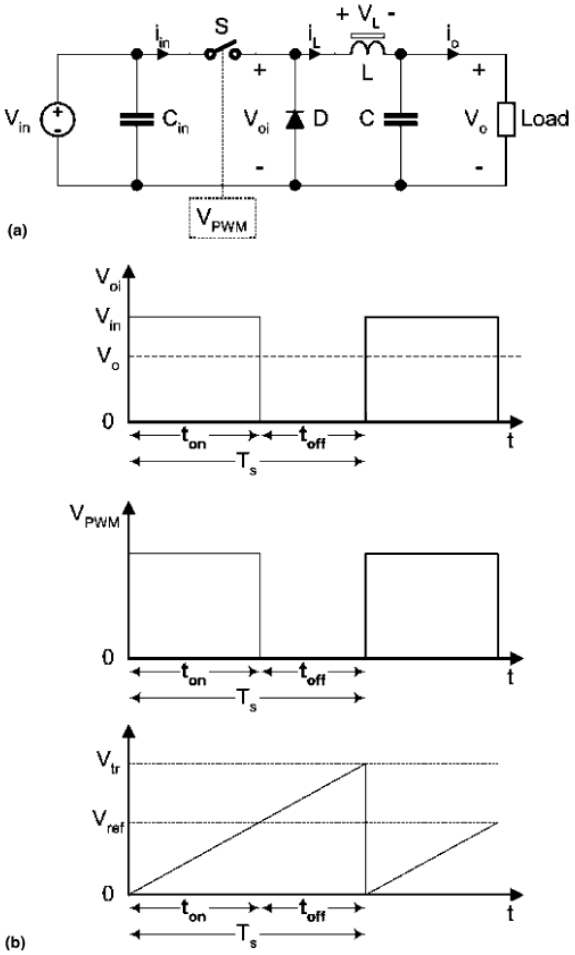


Fig. 2 PWM control of a buck-type DC/DC converter: (a) power converter diagram and (b) associated waveforms.

An N-bit value, corresponding to the desired duty cycle value, is compared with the value of an N-bit counter running with clock frequency $f_{clock}$. The comparator output is used to trigger a toggle register, producing a PWM output signal with adjustable duty cycle. Using an N-bit resolution, resulting in $2^N$ different duty cycle states, the clock frequency, $f_{clock}$, is related to the PWM output wave frequency, $f_{PWM}$, as follows:

$$f_{PWM} = \frac{f_{clock}}{2^N}$$

If the PWM generator is implemented in software, then a number of instructions is required, each one executed in state times which are multiples of the microcontroller clock period, also resulting in a low PWM frequency and/or resolution.

A Digital to Analog converter is used to convert a digital word to the corresponding analog reference voltage, which is then compared with a triangular wave in order to produce the PWM signal [8].

This method has the following disadvantages: (a) the PWM generation unit is sensitive to noise and component value variations and
(b) the system cost is increased because additional components are required.

The development of field programmable gate array (FPGA) and complex programmable logic device (CPLD) ICs provides an alternative solution for the implementation of digital power converter control units. They have the advantage of flexibility due to their reprogramming capability, while their operating frequency can be as much as hundreds of MHz. FPGAs have been used in power electronics applications for the implementation of complicated control schemes, such as fuzzy logic control of a DC/DC converter [12] and deadbeat control of a three-phase DC/AC inverter [13].

The PWM signals produced feature frequencies which range from 9 kHz up to 31.25 kHz, but their operation at higher frequencies has not been investigated. The implementation of FPGA-based digital control schemes is economically feasible when applied to power converters of moderate power level (e.g. over 100 W) so the proposed system is designed according to the counter- based architecture. Additionally, the counter-based architecture has the advantage of lower area consumption, which is critical in case that complex control schemes with large area requirements are to be implemented in the same FPGA or CPLD IC. The proposed PWM generation unit is based on a specially designed, synchronous binary counter, resulting in maximum PWM frequencies up to 3.985 MHz with a duty cycle resolution of 1.56%, while the PWM unit can be easily interfaced to a microcontroller or DSP system.

The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required.

## 3 THE PROPOSED PWM ARCHITECTURE

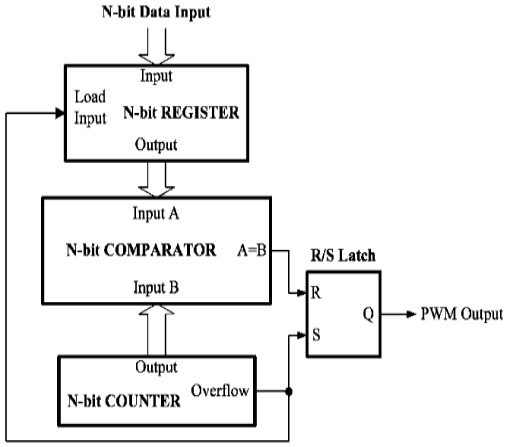


Fig. 3. Block diagram of the proposed PWM generator

The system input is an N-bit data word, corresponding to the desired PWM duty cycle value, so that it can be easily interfaced to a microcontroller unit I/O port pins. The N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit free-running synchronous counter, by means of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition at the end of a PWM period. Also, the counter overflow signal is used to load the N-bit data input to the input register, so that the PWM output duty cycle change is performed at the new PWM wave period in order to avoid any frequency and/or phase jitter of the output waveform. The duty cycle is given from the following equation:

$$D = \frac{\text{Data\_Value}}{2^N}$$

where Data_Value is the input data word integer value.

If an 8-bit input is used, then the duty cycle is in the range $0 \le D \le {}^{255}/_{256} = 99{:}6\%$. Since the PWM duty cycle has $2^N$ different states, the generator resolution, ◎ , is defined as

$$\alpha = \frac{1}{2^N} \cdot 100\%$$

In order to achieve high PWM frequencies, resulting in high clock rates, a fast counter is required. Synchronous counters have the inherent characteristic that the latency related to the state decoding bounds the maximum permissible clock frequency, thus an alternative design method has to be introduced. The block diagram of the fully synchronous free-running counter implemented is shown in Fig. 4 and the corresponding waveforms in Fig. 5. The counter has been built around: (a) toggle flip-flops, $T_0 \ldots T_{N-1}$, corresponding to the counter output bits C(0) . . . C($N$-1) and (b) a combination of D-type flipflops, $D_1 \ldots D_{N-1}$, with outputs $Q(1) \ldots Q(N-2)$ and AND gates, $G_1 \ldots G_{N-1}$, comprising the state decode logic within the counter. All flip-flops are clocked with a common clock signal, $f_{clock}$ and if a toggle flip-flop input, EN, is set, then its output, $T$, is toggled at the next clock pulse. Thus, each D-type flip-flop, $D_i$, is used to prepare the subsequent toggle flip-flop, $T_{i+1}$, output state change, by setting the corresponding input one cycle before this change must take place. Also, each AND gate, $G_i$, is used to predict the C($i$ + 1) counter output state change two clock cycles before the clock cycle that this change must be executed. Finally, the counter ''Overflow'' signal is produced by the $D_{N-1}$ flip-flop at the end of the PWM period and is used to load the new duty cycle value to the PWM generator input register.

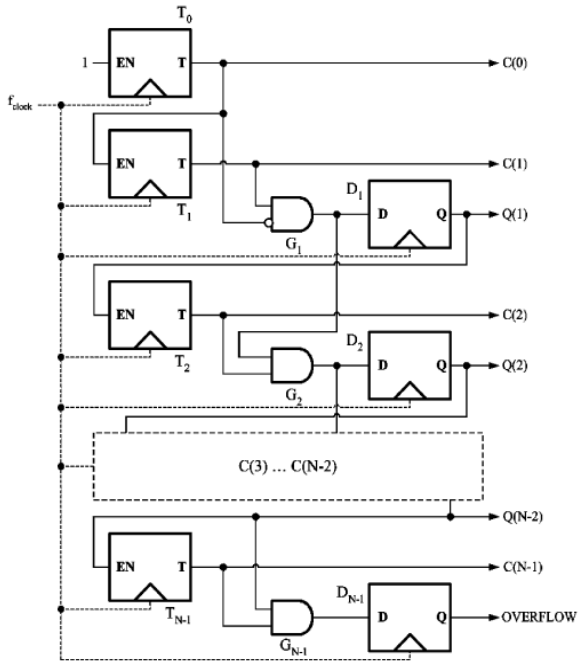


Fig. 4. Block diagram of the counter

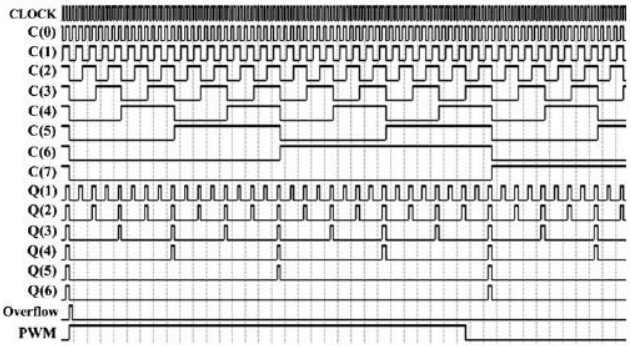


Fig. 5. Timing Waveforms of the Counter

If a Xilinx VIRTEX or SPARTAN-II FPGA is used, then the on-chip delay-locked-loops can be used to multiply

the input clock and eliminate any clock delay within the device.

## 4 SIMULATION RESULTS

A software program using the VHDL language was developed, for synthesizing the architecture, using the Xilinx Foundation software v3.1. The Xilinx Software timing analyzer is used for various devices manufactured by Xilinx. The maximum clock speed is increased if the PWM resolution is reduced, because of the delay reduction associated with the counter internal logic.

Observation of the results show that PWM frequencies up to 3.985 MHz can be produced using the proposed design method with a duty cycle resolution of 1.56%, which is adequate for a number of applications such as motor control, renewable energy systems control, etc. A plot of the resulting maximum PWM frequency versus the FPGA or CPLD device type for duty cycle resolution values of 0.39%, 0.78% and 1.56%, respectively, is presented in Fig. 6.

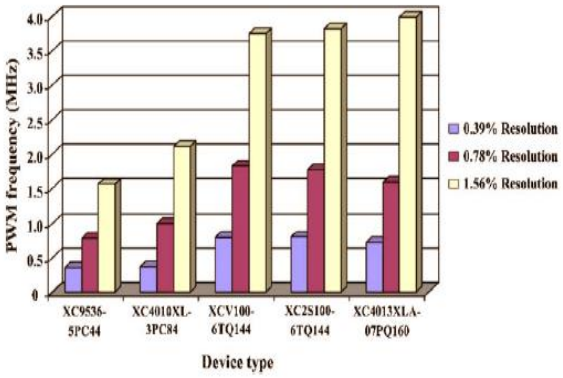


Fig. 6. The post-layout resulting maximum PWM frequency versus the FPGA or CPLD device type for various duty cycle resolution values.

It is observed that the PWM frequency depends on the target device speed grade and the duty cycle resolution. The FPGA or CPLD device type is selected according to the digital control system implementation area and cost requirements. The desired PWM frequency can be achieved with high (worse) duty cycle resolution for the selected FPGA or CPLD IC, then duty cycle dithering techniques can be easily combined with the proposed methodology in order to enhance the resolution of the resulting duty cycle values [19].

The timing analyzer is rather conservative and the maximum clock frequency that can be achieved using the proposed system, under practical conditions, can be considerably higher compared to the simulation results. Thus, the post-layout timing results are frequently used to analyze and demonstrate the performance of FPGA designs [20]. Furthermore, the maximum clock frequency can be further increased using manual placement techniques, during the device configuration stage [21].

The oscilloscope waveforms of the PWM output for 86.71% and 36.71% duty cycle values are shown in Fig. 7 (a) and (b), respectively. The output waveform for a 7-bit data input implementation, resulting in a 93.75 kHz PWM frequency, is shown in Fig. 8(a). The PWM duty cycle is externally adjusted to 24.25%. The corresponding output waveform for a 6-bit data input implementation is shown in Fig. 8(b). The resulting PWM frequency in this case is 187.5 kHz, while the duty cycle is adjusted to 40.6%.

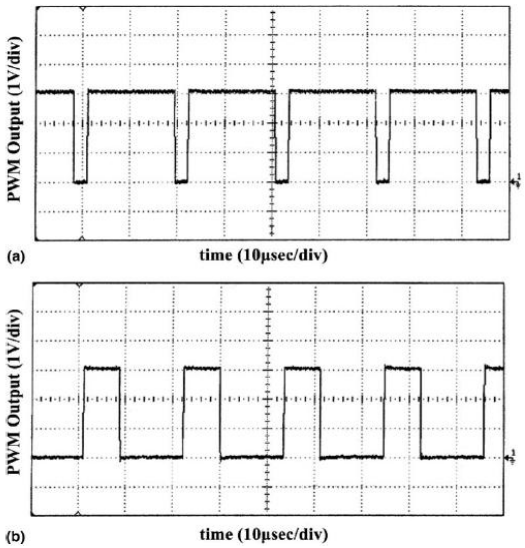


Fig. 7. Oscilloscope waveforms of the PWM output for various duty cycle values: (a) 86.71% and (b) 36.71%.

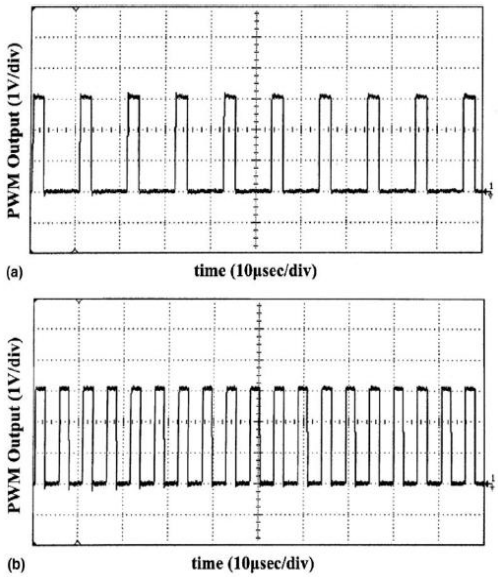


Fig. 8. Oscilloscope waveforms of the PWM output for two different data input length implementations: (a) 7-bit input and (b) 6-bit input.

## 5 CONCLUSION

In this paper, a high-frequency PWM generator architecture for power converter control, using FPGA

and CPLD ICs, has been presented. The proposed architecture is based on a special design synchronous binary counter and can be easily interfaced to a microcontroller or DSP system. The post-layout timing simulation results prove that using proposed method, PWM frequencies up to 3.985 MHz can be produced with a duty cycle resolution of 1.56%, which is adequate for most applications. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required. The selection of the target device depends on the system cost and resolution requirements.

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